



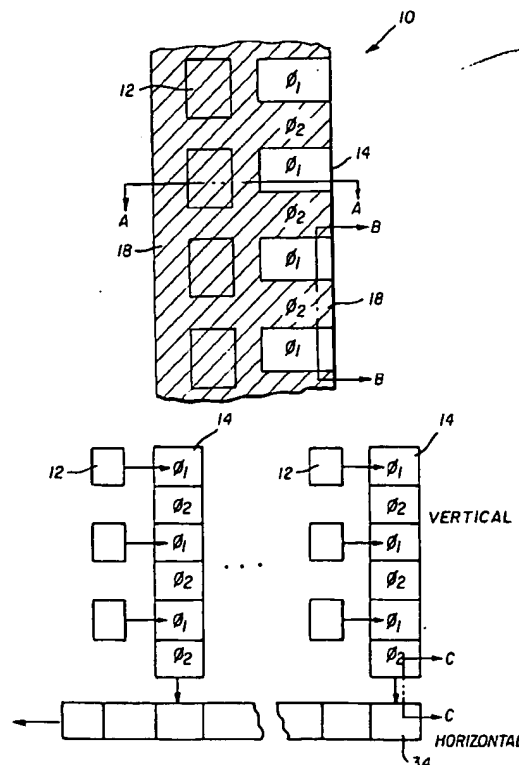
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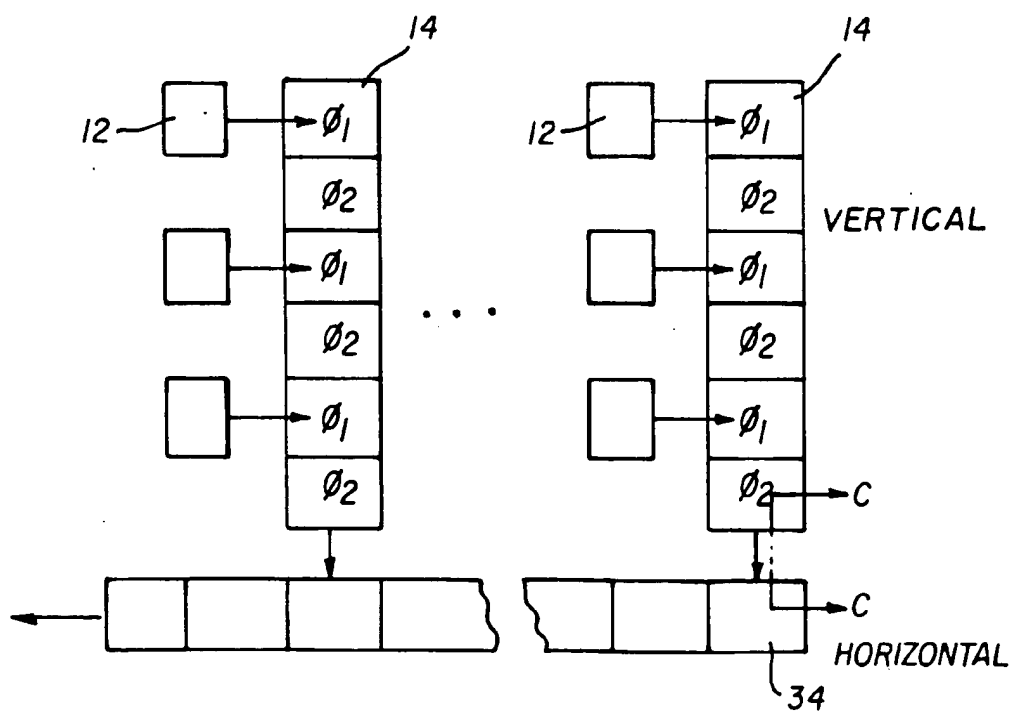
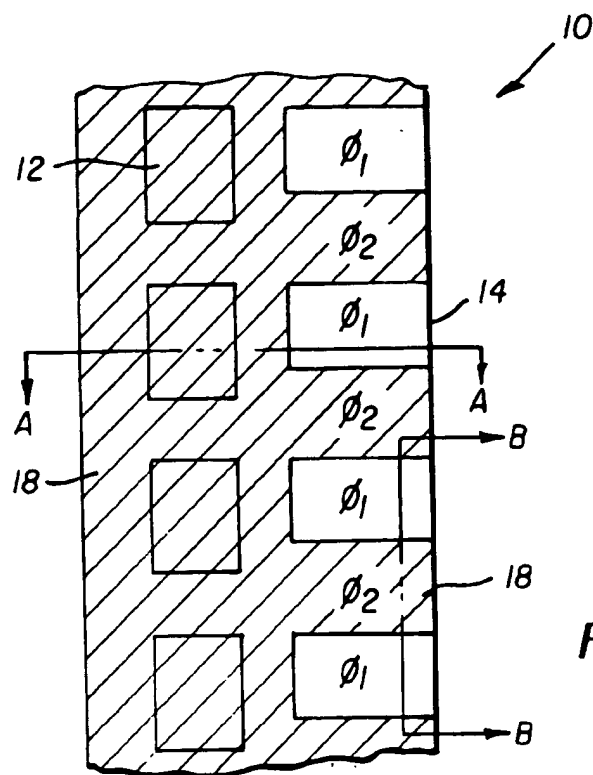
United States Patent [19]
Anagnostopoulos[11] **Patent Number:** **5,814,810**[45] **Date of Patent:** **Sep. 29, 1998****[54] INTERLINE SENSOR EMPLOYING
PHOTOCAPACITOR GATE****[75] Inventor:** Constantine N. Anagnostopoulos,
Mendon, N.Y.**[73] Assignee:** Eastman Kodak Company, Rochester,
N.Y.**[21] Appl. No.:** 933,304**[22] Filed:** Sep. 18, 1997**Related U.S. Application Data****[62]** Division of Ser. No. 636,434, Apr. 23, 1996.**[60]** Provisional application No. 60/005,395 Oct. 4, 1995.**[51] Int. Cl. ⁶** **H01L 27/00; G11C 19/28;**
..... **H03K 23/46****[52] U.S. Cl.** **250/208.1; 377/60; 257/217****[58] Field of Search** **250/208.1; 377/60-63;**
..... **257/217, 247, 232****[56] References Cited****U.S. PATENT DOCUMENTS**

4,908,518	3/1990	Losee et al.	257/232
5,051,832	9/1991	Losee et al.	257/232
5,060,245	10/1991	Nelson	377/60
5,235,198	8/1993	Stevens et al.	257/232
5,256,891	10/1993	Losee et al.	257/233
5,625,210	4/1997	Lee et al.	257/292

Primary Examiner—Stephone B. Allen**Attorney, Agent, or Firm**—James D. Leimbach**[57] ABSTRACT**

An interline sensor is constructed using photocopacitors. The vertical shift register of the interline sensor is operated in a uniphase mode, i.e., holding one of the two phase ($\phi 2$) at a D.C. potential while fluctuating the other phase ($\phi 1$) between a voltage that is sufficiently above and below that D.C. potential to facilitate transfer of charge from one phase to the next. The uniphase mode is facilitated by a single electrode, an indium tin oxide electrode, that covers both the phase that is held at a constant D.C. potential and the photodetector having photocopacitor charges. The charges are transferred from the photocopacitors to the vertical shift register by a third level clock into ($\phi 1$) adjacent the photodetectors utilizing the same ITO electrode for phase 2 of both the vertical and horizontal CCD shift registers is also proposed. Furthermore, to avoid having to separate the ITO electrode into the photocopacitor gate and the phase 2 gate, it is proposed that no cut is made within the electrode and that the vertical register be operated in the uniphase mode. That is the ITO electrode is biased to voltage of about -5 volts. It is important that the photocopacitor accumulation potential be about -4 volts so that its surface remains low. The horizontal register can be operated in the standard two phase mode so that the electrical noise in the video signal is maintained at a low level.

6 Claims, 4 Drawing Sheets



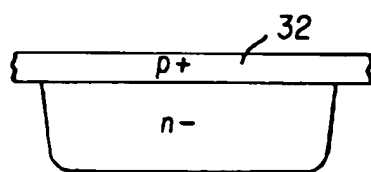


FIG. 3

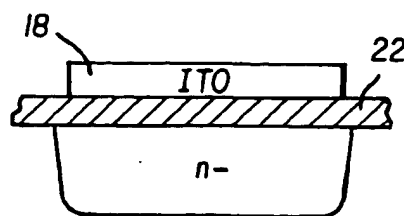


FIG. 2

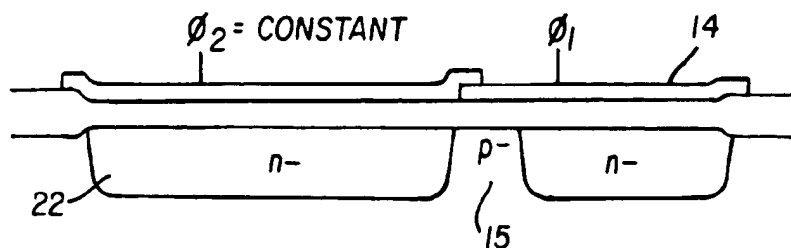


FIG. 4a

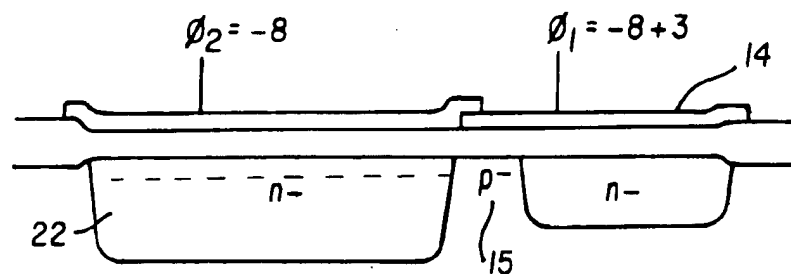


FIG. 4b

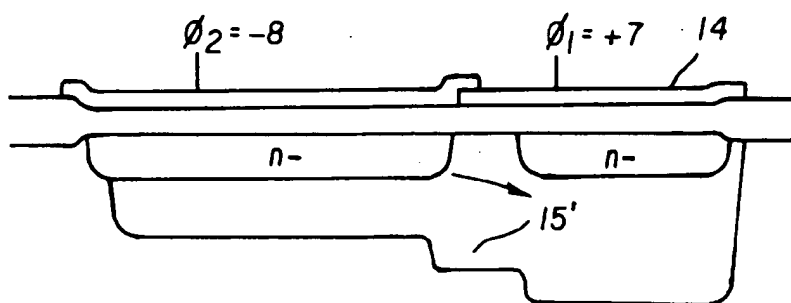


FIG. 4c

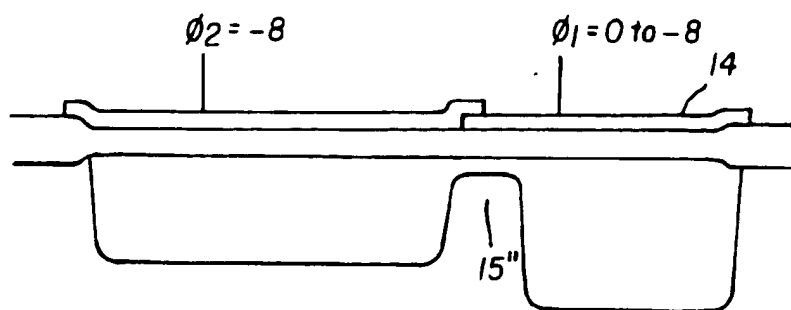


FIG. 4d

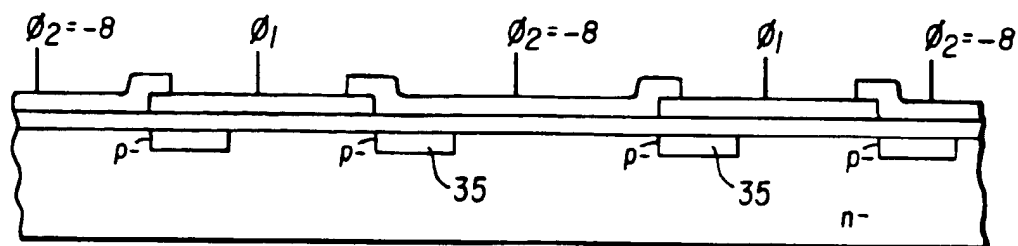


FIG. 5a

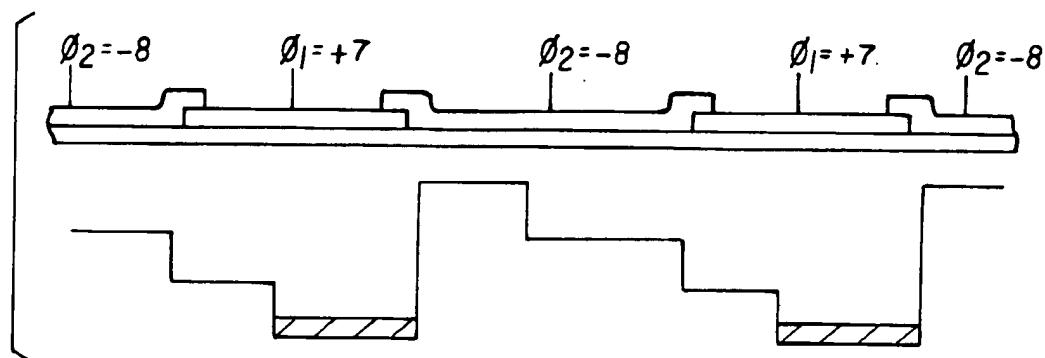


FIG. 5b

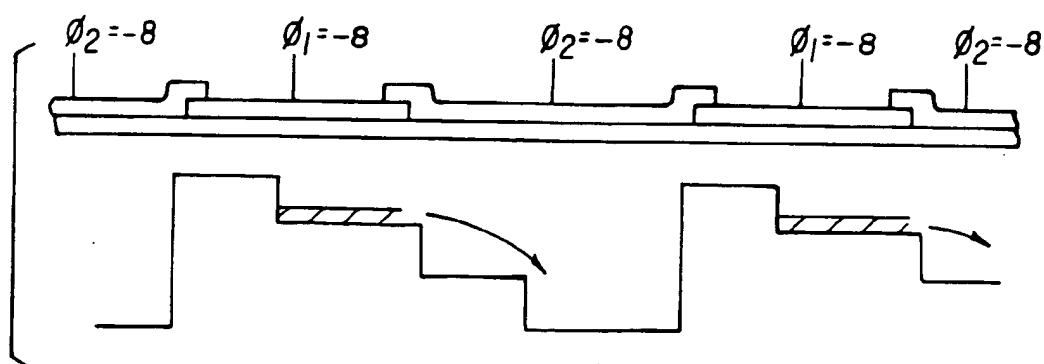


FIG. 5c

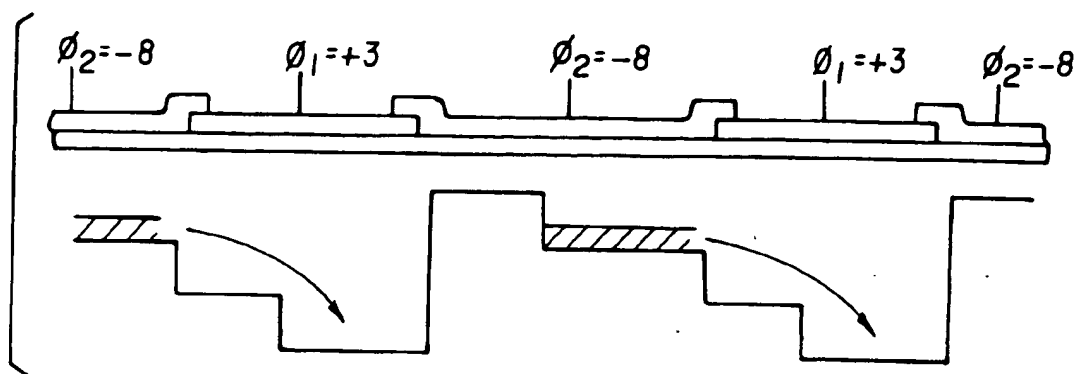


FIG. 5d

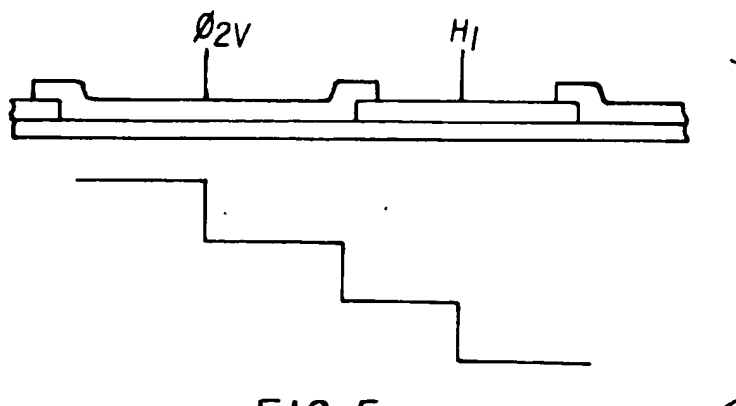


FIG. 5e

INTERLINE SENSOR EMPLOYING PHOTOCAPACITOR GATE

This is a Divisional of U.S. application Ser. No. 08/636, 434, filed 23 Apr. 1996, which is based upon Aug. 24, 1998 Provisional application Ser. No. 60/005,395, filed 04 Oct. 1995.

FIELD OF INVENTION

The invention relates generally to the field of charge coupled devices, and more specifically, the invention relates to interline sensors having a photocapacitor in place of a pinned photodiode and an indium-tin-oxide electrode covering the photocapacitor.

BACKGROUND OF THE INVENTION

There are numerous devices within the prior art that describe uniphase and virtual phase. While uniphase devices within the prior art are very commonly referred to as virtual phase devices, there are basic differences in the two terms. Devices can meet the criteria both uniphase and virtual phases. The prior art device in U.S. Pat. No. 4,229,752 issued to Hyneccek on Oct. 21, 1980 discloses a continuous conductive layer, such as tin oxide, to form the single-phase clock electrode as shown in FIG. 6e of that patent (Col. 6, lines 24-28). A smaller voltage swing is sufficient to cause propagation of the signal charge packets to successive cells (Col. 6, lines 37-39). The invention can be used in CCD imagers including linear shift registers (Col. 6, lines 25-65). However, these devices are not interline devices. Moreover, no technique is disclosed to provide an ITO electrode that is placed over both the photodetector elements as well as a portion of a shift register.

Another prior art device is described in U.S. Pat. No. 4,814,844 issued to Bluzer on Mar. 21, 1989, which describes split two-phase CCD clocking gates held at constant potential with a first phase clock signal and second phase clock signal being adjusted to move charge from beneath the first phase electrode to beneath the second phase electrode (Col. 5, lines 9-20). More than two clock gate phase, e.g., three, four, etc. may be utilized (Col. 5, lines 41-43). While virtual two-phase devices are described, no disclosure is made of employing a uniphase effect to transfer charge from the photodetector elements themselves. Furthermore, no disclosure is made of employing a photocapacitor as the photodetector element.

U.S. Pat. No. 4,732,868 issued to Nichols on Mar. 22, 1988, commonly assigned with the present invention, discloses a uniphase CCD employing a gate conductor of tin-doped indium oxide (Col. 4, lines 48-51). The CCD is used in imaging devices, such as the frame transfer type (Col. 4, lines 52-54). A gate electrode can be deposited over the gate oxide as seen in FIG. 7 (Col. 4, lines 44-45). However, Nichols, does not teach any usefulness of employing a photocapacitor as the photodetector element or for employing a contiguous ITO electrode over both the photodetector and the adjacent shift register.

Still another prior art device is discussed in U.S. Pat. No. 5,210,049 which issued to Anagnostopoulos on May 11, 1993, and commonly assigned with the present invention, discloses an image sensor having a charge-coupled device shift register and at least one photocapacitor (Col. 2, lines 28-30). However, a single electrode covering both a portion of the vertical shift register and the photodetector, as required for true two-phase operation, is not taught.

Furthermore, prior art devices employing pinned photodiode technology have disadvantages such as process com-

plexity. While pinned photodiodes have advantages for dark current characteristics because the dark current is low because the surface states are passivated by the shallow boron implants. However, the very shallow, heavy boron implants that can not be annealed properly (thus producing defects) and parasitic barriers between the photodiode and the vertical shift register, again arising because of the high boron dose pinning layer.

Pinned photodiodes also have good blue light response. This is an advantage over photocapacitor technology employing polysilicon electrodes.

From the foregoing discussion it should be apparent that there is a need for an image sensor that provides a true uniphase mode of operation, including transfer of charge from the photodetector area to a phase of the vertical shift register and also teaches the use of a photocapacitor as the photodetector element.

SUMMARY OF THE INVENTION

The present invention is directed to overcoming one or more of the problems set forth above to provide true uniphase operation. In progressive scan interline sensors it is proposed that the photodiode be replaced by a photocapacitor with ITO gate electrode.

An interline sensor is constructed using photocapacitors. The vertical shift register of the interline sensor is operated in a uniphase mode, i.e., holding one of the two phases ($\phi 2$) at a D.C. potential while fluctuating the other phase ($\phi 1$) between a voltage that is sufficiently above and below that D.C. potential to facilitate transfer of charge from one phase to the next. The uniphase mode is facilitated by a single electrode that covers both the phase that is held at a constant D.C. potential and the photodetector having photocapacitor charges. The single electrode in the preferred embodiment is an indium tin oxide electrode. The charges are transferred from the photocapacitors to the vertical shift register by a third level clock into $\phi 1$ adjacent the photodetectors.

It is also proposed that the same ITO electrode be utilized for phase 2 of both the vertical and horizontal CCD shift registers. Furthermore, to avoid having to separate the ITO electrode into the photocapacitor gate and the phase 2 gate, it is proposed that no cut is made within the electrode and that the vertical register be operated in the uniphase mode. That is the ITO electrode is biased to voltage of about -5 volts. It is important that the photocapacitor accumulation potential be about -4 volts so that its surface remains accumulated at all times and thus the dark current remains low. The horizontal register can be operated in the standard two phase mode so that the electrical noise in the video signal is maintained at a low level.

The above and other objects of the present invention will become more apparent when taken in conjunction with the following description and drawings wherein identical reference numerals have been used, where possible, to designate identical elements that are common to the figures which illustrate an interline sensor constructed to operate in a uniphase mode having at least one vertical shift register, the vertical shift registers being constructed as two-phase shift registers with a plurality of photodetectors adjacent each of the vertical shift registers, a barrier region between each photodetectors and its respective vertical shift register, single phase means for allowing the transfer of charge from the photodetectors to the vertical shift registers to operate in a uniphase mode by adjusting only one of the phases; and at least one horizontal shift register.

ADVANTAGEOUS EFFECT OF THE INVENTION

The present invention has the following advantages. It provides a reduction of dim point defects to a level seen in

full frame ITO sensors. Further, it provides a reduction in the number of fabrication steps required and relaxes the process tolerances. An increased yield is seen as well as a process consolidation. These advantages are achieved with no resulting loss in quantum efficiency as compared to photodiode detectors including the blue region of the spectrum because of the usage of ITO electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a is a diagram of an interline sensor constructed in accordance with the present invention such that the photodetectors are made using photocapacitors;

FIG. 1b is a diagram illustrating the interline sensor configuration that is employed by the present invention;

FIG. 2 is a diagram of a photocapacitor as envisioned by the present invention;

FIG. 3 is a pinned photodiode employed by the prior art as a photodetector;

FIG. 4a is a cross sectional diagram taken along the line A—A of FIG. 1 through the photocapacitor and the $\phi 1$ of the vertical shift register;

FIG. 4b is the cross sectional diagram of FIG. 4a where the potential levels of $\phi 1$ and $\phi 2$ are configured for integration mode;

FIG. 4c is the cross sectional diagram of FIG. 4a where the potential levels of $\phi 1$ and $\phi 2$ are configured for transfer mode;

FIG. 4d is the cross sectional diagram of FIG. 4a where the potential levels of $\phi 1$ and $\phi 2$ are configured for clock out mode;

FIG. 5a is a cross sectional diagram taken along the line B—B of FIG. 1 where $\phi 1$ and $\phi 2$ are at a constant potential an associated potential diagram;

FIG. 5b is the cross sectional diagram of FIG. 5a where $\phi 1$ and $\phi 2$ are configured for transferring all charge within the photodiodes to $\phi 1$ under application of a +7 volt third level clock;

FIG. 5c is a cross sectional diagram of FIG. 5a where $\phi 1$ and $\phi 2$ are configured to transfer charge from beneath $\phi 1$ to beneath $\phi 2$;

FIG. 5d is the cross sectional diagram of FIG. 5a where $\phi 1$ and $\phi 2$ are configured to transfer charge from beneath $\phi 2$ to beneath $\phi 1$;

FIG. 5e is the cross sectional diagram of FIG. 1b along line VV where $\phi 2$ and H1 are configured to transfer charge from the vertical shift register to the horizontal shift register with an associated potential diagram.

DETAILED DESCRIPTION OF THE INVENTION

I have discovered that an interline sensor 10, as shown in FIG. 1a and FIG. 1b, can be constructed with photodetectors 12 made using a photocapacitor 22, as seen in FIG. 2. This differs from the pinned photodiode 32 employed by the prior art, as shown in FIG. 3. By employing a photocapacitor 22 in place of a pinned photodiode 32, the interline sensor 10 can then have the adjacent vertical shift register 14 operated in a uniphase mode, i.e. holding one of the two phases ($\phi 2$ as shown FIG. 1) at a D.C. potential while fluctuating the other phase ($\phi 1$ as shown in FIG. 1) between a voltage that is sufficiently above and below that D.C. potential to facilitate transfer of charge from one phase to the next. The present invention envisions that this transfer be accommodated by a single electrode material 18 that covers both the photodetectors 12 and the phase held at a constant potential ($\phi 2$).

In the preferred embodiment an INDIUM-TIN-OXIDE (ITO) electrode material is employed as electrode 18 covering both the phase that is held at a constant D.C. potential and the photodetectors 12 which are photocapacitors 22. Charges are transferred from the photocapacitor 22 to the vertical shift register 14 by a third level clock into $\phi 1$ adjacent the photodetectors 12.

Prior art devices employ as the photocapacitors (ITO electrode) in place of the pinned photodiode without the provision of a contiguous ITO electrode over the photodetector and any phase of the vertical shift register.

Uniphase devices are known as are virtual phase devices (Texas Instruments) that operate in a manner similar to a uniphase device. However, these devices are not interline devices and do not provide for the ITO electrode to be placed over both the photodetectors' elements as well as a portion of a shift register.

Referring now to FIGS. 4a-4d, FIG. 4a is a cross sectional diagram taken along the line A—A of FIG. 1 with a corresponding potential diagram for $\phi 1$ and the photocapacitor 22 operated under control of the $\phi 2$ phase. Here, both the photocapacitor 22 and the $\phi 1$ area of the vertical shift register 14 have n- area that are separated from each other by the barrier region 15 which is juxtapositioned beneath the edge of the $\phi 1$ electrode. Barrier region 15 is a p- doped area that allows the present invention to operate in the context of the preferred embodiment as explained, herein. FIG. 4a illustrates a cross sectional view of the device as taken along the line AA of FIG. 1a. Referring to FIG. 4b, $\phi 2$ is held at a constant potential of -8 volts and $\phi 1$ is held at a level that does not overcome the potential barrier 15. This level can fluctuate within the preferred embodiment from +3 to -8 volts (a +7 volt is necessary to overcome barrier region 15). This allows barrier region 15 to provide separation between the photocapacitor 22 and the vertical shift register 14 as shown in FIG. 4a.

FIG. 4b is the cross sectional diagram of FIG. 4a where the levels of $\phi 1$ and $\phi 2$ both have a level -8 volts applied for operation in the integration mode. Here, barrier 15 still provides the separation potential between the photocapacitor region 22 beneath the $\phi 2$ electrode and the $\phi 1$ phase of the vertical shift register 14. Charge will accumulate in the photocapacitor region 22 for a predetermined periods of time until transfer to the vertical shift register.

FIG. 4c illustrates the voltage levels of the $\phi 1$ phase of the vertical shift register and the $\phi 2$ electrode configured for transfer mode wherein charges stored within the photocapacitor 22 are transferred to the $\phi 1$ phase of the vertical shift register 14. Here, while $\phi 2$ remains at the integration mode level of -8 volts, the $\phi 1$ phase is placed at a +7 volt level. This facilitates the transfer of charge from the area $\phi 2$ beneath the photocapacitor 22, over the barrier potential 15, to the $\phi 1$ phase of the vertical shift register 14.

FIG. 5a is a cross sectional diagram of the vertical shift register 14 taken along the line B—B of FIG. 1. The cross sectional diagram shown in FIG. 5a both phases placed at the D.C. level, which is -8 volts. This equipotential on either side of barrier 35 prevents charge from transferring between the two phases.

FIG. 5b illustrates the transfer of charge within the photocapacitors to the $\phi 1$ phase of the vertical shift register by the application of a third level clock, here seen at a +7 voltage level, to the $\phi 1$ electrode. The effect of the third level clock is seen by referring to the potential diagram. Here, the potential well create by the third level clock is readily apparent, as it causes the charges beneath the of the photo-

capacitor (not shown) to step into the deeper potential well beneath the $\phi 1$ electrode. The area beneath the vertical shift register $\phi 2$ electrode remains at a level D.C. level of -8 volts that was used to transfer charge from the photocapacitor.

FIG. 5c is the cross sectional diagram of FIG. 5a where $\phi 1$ and $\phi 2$ are configured to transfer charge through the vertical shift register. Here, the third level clock shown in FIG. 5b is removed and a -8 volt level is placed on the $\phi 1$ electrode. This allows the well beneath the $\phi 1$ to collapse and the charges formerly in beneath the $\phi 1$ electrode to fall to the area contained beneath the $\phi 2$ electrode. Barrier 35 is a p- doped area that prevents the charge from traversing the vertical shift register 14 opposite the desired path. In this manner charge is moved down the vertical shift register 14 and into the horizontal shift register 34. The line contained within the vertical shift registers 14 is thereby, transferred out to the horizontal shift register.

FIG. 5d is the cross sectional diagram of FIG. 5a where the voltages applied to the $\phi 1$ and $\phi 2$ phases to allow transfer of charge through next phase of the vertical shift register. $\phi 1$ is placed at a level of +3 volts while $\phi 2$ remains at a -8 volt level resulting in a transfer of charge as indicated by the accompanying potential diagram. Taken in conjunction with FIG. 5c a transfer of charge through a complete stage of the vertical shift register has completed.

FIG. 5e is cross sectional diagram of FIG. 1b taken along the line CC to illustrate the transfer of charge from the vertical shift register to the horizontal shift register. The transfer from the vertical shift register to the horizontal shift register occurs from charge stored within the last $\phi 2$ phase of the vertical shift register and is transferred to the $\phi 1$ phase of the horizontal shift register.

There are limitations to the present invention. A resulting increase in CCD dark current occurs that can be eliminated by operating phase 2 in accumulation, i.e. clock phase 2 of the vertical shift register at between -10 and -5 volts.

It is also proposed that the same ITO electrode be utilized to for phase 2 of both the vertical and horizontal CCD shift registers. Furthermore, to avoid having to separate the ITO electrode into the photocapacitor gate and the phase 2 gate, it is proposed that no cut is made within the electrode and that the vertical register be operated in the uniphase mode. That is the ITO electrode is biased to voltage of about -5 volts. It is important that the photocapacitor surface also remains in accumulation at all times and thus the dark current remains low. The horizontal register can be operated in the standard two phase mode so that the electrical noise in the video signal is maintained at a low level.

It is also envisioned that the photocapacitor of the present invention be employed in multi-phase devices of two or more phases. In such an embodiment there would be an electrical separation (not shown) between the photocapacitor electrode and the electrodes of the vertical shift register. Also the vertical shift register could be operated in multiple phases. Such embodiments would comprises either polysilicon or ITO as photocapacitor elements. Using an ITO electrode would yield better response in the blue region of the spectrum. Whereas polysilicon is a more commonly used material due to being more compatible with silicon based devices.

The invention has been described with reference to a preferred embodiment. However, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention.

Parts List:

- 10 interline sensor
- 12 photodetectors
- 14 vertical shift register
- 15 p- barrier between photocapacitor and the vertical shift register
- 18 side electrode material
- 22 photocapacitor
- 32 photodiode
- 34 horizontal shift register
- 35 p- barrier in vertical shift register between phases

I claim:

1. An interline sensor comprising:
 - a silicon substrate;
 - at least one vertical shift register within the substrate, the vertical shift register having a plurality of electrodes for shifting charge through the electrode;
 - a plurality of photodetectors within the substrate adjacent the vertical shift register, each photodetector comprising a photocapacitor;
 - a barrier region between each photodetector and the vertical shift register;
 - means for applying a first potential level and a second potential level to the electrodes of the vertical shift register;
 - single phase means for allowing the transfer of charge from the photocapacitor to the vertical shift register in a uniphase mode by adjusting the potential applied to only one of the electrodes of the vertical shift register;
 - a third level clock operatively coupled to one phase of vertical shift register for each photocapacitor; and
 - at least one horizontal shift register operatively coupled to receive charge from the vertical shift register.
2. The sensor of claim 1 wherein the sensor further comprises an electrode as part of the photocapacitor that is biased at a potential that is sufficient to passivate interface states within the photocapacitor.
3. The sensor of claim 2 wherein the electrode further comprises a polysilicon electrode.
4. The sensor of claim 2 wherein the electrode further comprises an ITO electrode.
5. The sensor of claim 3 where the electrode is electrically isolated from the vertical shift register electrodes.
6. The sensor of claim 4 wherein the ITO electrode has a first portion over the photodetector and a second portion over the one phase of the vertical shift register with first portion and the second portion formed by a single contiguous ITO layer.

* * * * *